

### **OpenACC programming** on NVIDIA GPUs

#### Epicure hackathon @ CINECA, Casalecchio di Reno (BO) Italy 28-31 October 2024







This project has received funding from the High Performance Computing Joint Undertaking under grant agreement No 101139786

# Why OpenACC?

#### Incremental approach

The runtime can handle data movements, compiler optimizes the offload for the underlying hardware

#### Avoid source code duplication

Based on compiler directives, acc activated via compilation flags

#### More portable

Supported also by AMD GPUs

```
< sequential code >
#pragma acc parallel loop
for( i = 0; i < N; i++)
          < loop code >
#pragma acc parallel loop
for( i = 0; i < N; i++ )</pre>
     < loop code >
}
< sequential code >
```



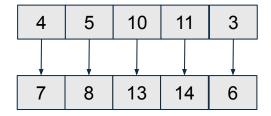
	1	
2 1 2 2		

# **Coding with OpenACC**

```
< cpu code >
#pragma acc parallel loop
for( i = 0; i < N; i++ )
        {
        output[i] = input[i] + scalar
}
< cpu code >
```

There must be no **data dependencies inside the loop** (each element computation at i is independent)

The compiler will compile the loop for the GPU



Each GPU thread will execute the operation on a subset of the iteration range

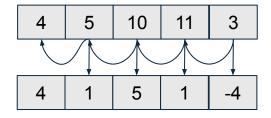
# **Data dependencies**

```
< cpu code >

#pragma acc parallel loop
for( i = 1; i < N; i++ )
        {
        output[i] = output[i-1] + scalar
}
< cpu code >
```

Not all loops are parallel!

If there dependencies between elements in the array, the GPU thread might access an element after it has changed



This provides wrong results

# **OpenACC** syntax

#### C/C++

#pragma acc directive clauses
<code>

#### Fortran

!\$acc directive clauses
<code>

A **pragma** in C/C++ gives instructions to the compiler on how to compile the code. Compilers that do not understand a particular pragma can freely ignore it.

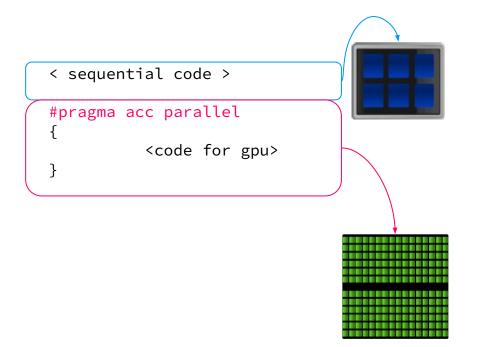
A *directive* in Fortran is a specially formatted comment that likewise instructions the compiler in it compilation of the code and can be freely ignored.

"*acc*" informs the compiler that what will come is an OpenACC directive

*Directives* are commands in OpenACC for altering our code.

*Clauses* are specifiers or additions to directives.

# The parallel directive



**parallel** instructs the compiler to **create parallel** *gangs* 

Gangs are **independent groups of** worker threads on the accelerator

The code contained within a parallel directive is executed redundantly by all parallel gangs

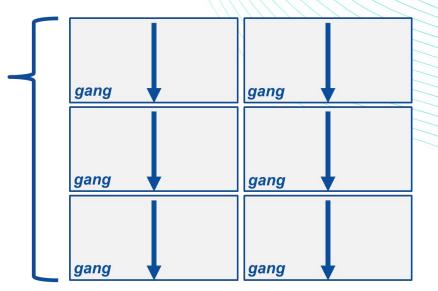
# The parallel directive

!\$acc parallel

< code for gpu >

!\$acc end parallel

The compiler will generate 1 or more parallel gangs, which execute redundantly.



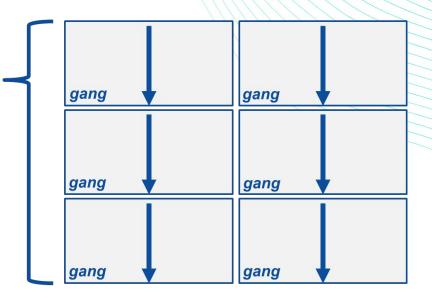
# The loop directive

#### !\$acc parallel

```
do i = 1, N
      < some operation >
end do
```

```
!$acc end parallel
```

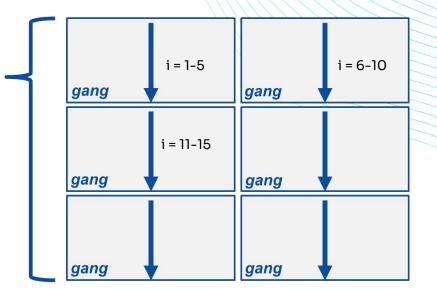
this way, the same loop is executed by each gang. We want to distribute loop iterations among gangs!



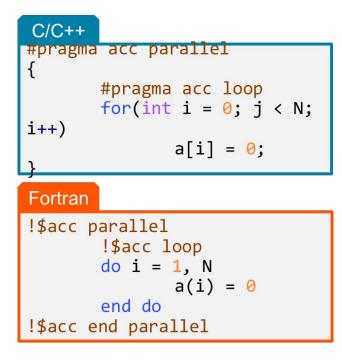
# The loop directive

!\$acc parallel
!\$acc loop
do i = 1, N
 < some operation >
end do
!\$acc end loop
!\$acc end parallel

the loop directive is used to distribute loop iterations among gangs



# The parallel loop directive



**parallel** marks a region of code where you parallel execution should occur

The **loop** directive is used to instruct the compiler to parallelize the iterations of the next loop to run across the parallel gangs

# The parallel loop directive

#### C/C++

#### Fortran

**parallel** marks a region of code where you parallel execution should occur

The **loop** directive is used to instruct the compiler to parallelize the iterations of the next loop to run across the parallel gangs

parallel loop can also be fused in a single direcive

# The kernels directive

```
#pragma acc kernels
{
   for(int i = 0; i < N; i++)
   a[i] = 0;
   for(int j = 0; j < M; j++)
   b[i] = 0;
}</pre>
```

```
!$acc kernels
a(:) = 1
b(:) = 2
c(:) = a(:) + b(:)
!$acc end kernels
```

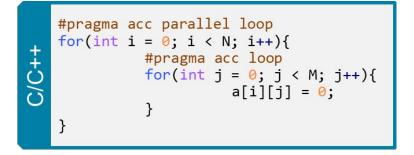
The **kernels** directive instructs the compiler to search for parallel loops in the code

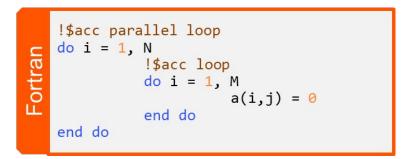
The compiler will analyze the loops and **parallelize those it finds safe** and profitable to do so

The kernels directive can be applied to regions containing multiple loop nests

#### Supports Fortran array syntax

# Loop nests





loop directives can be nested to parallelize multi-dimensional loops

This allows the compiler to implement more levels of parallelism, and increase performance, if resources are available

If more levels are not available, the inner loop directives will be ignored

The inner-most loop is not parallelizable, multiple threads could attempt to write to tmp  $\rightarrow$  we should expect to receive erroneous results

```
do k = 1, size
    do j = 1, size
    tmp = 0.0
    !$acc parallel loop
    do i = 1, size
        tmp = tmp + a(i,k) * b(k,j)
    end do
        c(i,j) = tmp
    end do
    end do
```

The inner-most loop is not parallelizable, multiple threads could attempt to write to tmp  $\rightarrow$  we should expect to receive erroneous results

To fix this, we should use the reduction clause

```
do k = 1, size
  do j = 1, size
  tmp = 0.0
  !$acc parallel loop reduction(+:tmp)
  do i = 1, size
    tmp = tmp + a(i,k) * b(k,j)
  end do
  c(i,j) = tmp
  end do
end do
```

The inner-most loop is not parallelizable, multiple threads could attempt to write to tmp  $\rightarrow$  we should expect to receive erroneous results

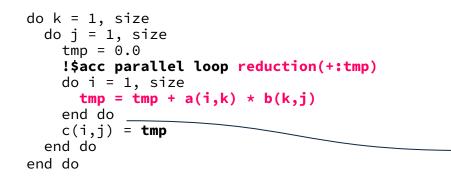
To fix this, we should use the reduction clause

```
do k = 1, size
  do j = 1, size
   tmp = 0.0
   !$acc parallel loop reduction(+:tmp)
   do i = 1, size
     tmp = tmp + a(i,k) * b(k,j)
   end do
   c(i,j) = tmp
  end do
end do
```

Each thread group will its own private copy of the reduction variable and perform a **partial reduction** on their loop iterations

The inner-most loop is not parallelizable, multiple threads could attempt to write to tmp  $\rightarrow$  we should expect to receive erroneous results

To fix this, we should use the reduction clause

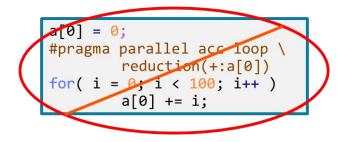


Each thread group will its own private copy of the reduction variable and perform a **partial reduction** on their loop iterations

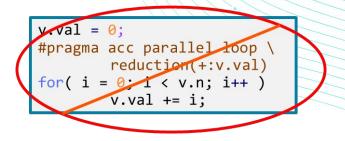
After the loop, a final reduction will be performed to produce a **single global result** 

# **Reduction operators**

Operator	Description	Example
+	Addition/Summation	reduction(+:sum)
*	Multiplication/Product	reduction(*:product)
max	Maximum value	reduction(max:maximum)
min	Minimum value	reduction(min:minimum)
ଷ	Bitwise and	reduction(&:val)
I.	Bitwise or	reduction( :val)
କ୍ଷ	Logical and	reduction(&&:val)
П	Logical or	reduction(  :val)



The reduction variable may not be an array element



The reduction variable may not be a C struct member, a C++ class or struct member, or a Fortran derived type member

# Sequential

```
#pragma acc parallel loop
for( i = 0; i < size; i++ )
    #pragma acc loop
    for( j = 0; j < size; j++ )
    #pragma acc loop seq
    for( k = 0; k < size; k++ )
        c[i][j] += a[i][k] * b[k][j];</pre>
```

The **seq clause will tell the compiler to run the loop sequentially** 

The compiler will parallelize the outer loops across the parallel threads, but each thread will run the inner-most loop sequentially

The compiler may automatically apply the seq clause to loops as well

## **Privatizations**

```
double tmp[3];
#pragma acc kernels loop private(tmp[0:3])
for( i = 0; i < size; i++ )
{
   tmp[0] = <value>;
   tmp[1] = <value>;
   tmp[2] = <value>;
}
// note that the host value of "tmp"
// remains unchanged.
```

Each thread can have a private copy of every variable

- private variables are uninitialized.
- firstprivate private values are initialized to the same value used on the host.

Unless doing a reduction, the value on the host outside the parallel region is unchanged

### **Privatizations**

```
double tmp[3];
#pragma acc kernels loop private(tmp[0:3])
for( i = 0; i < size; i++ ) {
    // the tmp array is private to each
iteration of the outer loop
    tmp[0] = <value>;
    tmp[1] = <value>;
    tmp[2] = <value>;
    #pragma acc loop
    for ( j = 0; j < size2; j++) {
        // but tmp is shared amongst the threads
        // in the inner loop
        array[i][j] = tmp[0]+tmp[1]+tmp[2];
    }
</pre>
```

Variables in **private** or **firstprivate** clause are private to the loop level on which the clause appears.

Private variables on an outer loop are shared within inner loops

## **Scalars**

By default, scalars are **firstprivate** when used in a parallel region and **private** when used in a kernels region.

Except in some cases, scalars do not need to be added to a private clause. These cases may include but are not limited to:

- 1. Scalars with global storage such as global variables in C/C++, Module variables in Fortran
- 2. When the scalar is passed by reference to a device subroutine
- 3. When the scalar is used as an rvalue after the compute region, aka "live-out"

Note that putting scalars in a private clause may actually hurt performance!

## **Collapse clause**

**collapse( N )** combines the next N tightly nested loops

Can turn a multidimensional loop nest into a single-dimension loop

This can be extremely useful for increasing **memory locality**, as well as creating larger loops to **expose more parallelism** 

```
#pragma acc parallel loop collapse(2)
for( i = 0; i < size; i++ ){
  for( j = 0; j < size; j++ ){
    double tmp = 0.0f;
    #pragma acc loop reduction(+:tmp)
    for( k = 0; k < size; k++ ){
      tmp += a[i][k] * b[k][j];
    }
    }
    c[i][j] = tmp;
}</pre>
```

# **Compiling for GPUs**

nvc -fast -acc -gpu=cc80,cuda12.3 -Minfo=accel main.c nvc++ -fast -acc -gpu=cc80,cuda12.3 -Minfo=accel main.cpp nvfortran -fast -acc -gpu=cc80,cuda12.3 -Minfo=accel main.f90

daxpy:

19, Generating NVIDIA GPU code

20, !\$acc loop gang, vector(128) ! blockidx%x threadidx%x

19, Generating implicit

copyout(y(1:2147483647),x(1:2147483647),d(1:2147483647)) [if not already present]

26, Generating NVIDIA GPU code

27, !\$acc loop gang, vector(128) ! blockidx%x threadidx%x

26, Generating implicit copyin(y(1:2147483647),x(1:2147483647)) [if not already present]

Generating implicit copyout(d(1:2147483647)) [if not already present]

# **Compiling for multicore**

nvc -fast -acc -ta=multicore -Minfo=accel main.c nvc++ -fast -acc -ta=multicore -Minfo=accel main.cpp nvfortran -fast -acc -ta=multicore -Minfo=accel main.f90

daxpy:

- 19, Generating Multicore code
  - 20, !\$acc loop gang
- 26, Generating Multicore code
  - 27, !\$acc loop gang

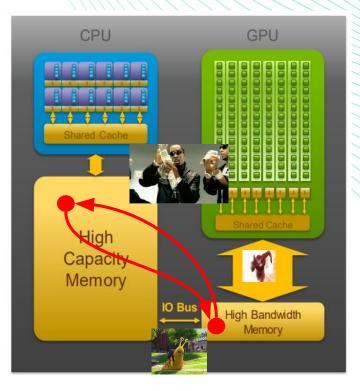
# Data management

Data must be visible on the **device** when running **parallel** code

Data must be visible on the **host** when running **sequential** code

When the host and device don't share memory, data movement must occur

To maximize performance, the programmer should avoid all unnecessary data transfers



do i = 1, N

D(i) = A \* X(i) + Y(i)

end do

!\$acc parallel do

do i = 1, N

D(i) = A \* X(i) + Y(i)

end do

!\$acc end parallel do

!\$acc parallel do

pgfortran -fast -acc -gpu=cc80,cuda12.3 -Minfo=accel -o
binary daxpy.f90
daxpy:

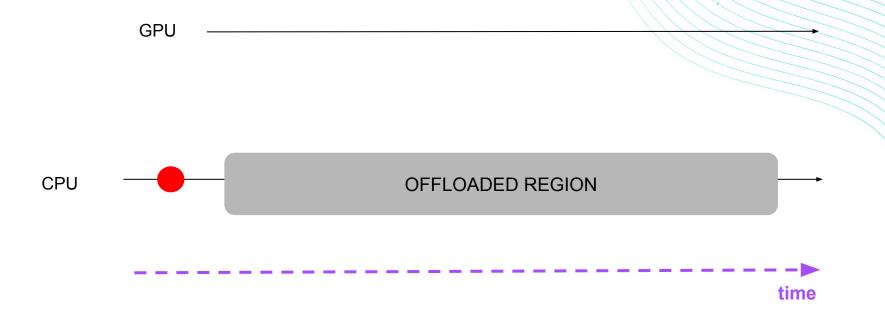
do i = 1, N

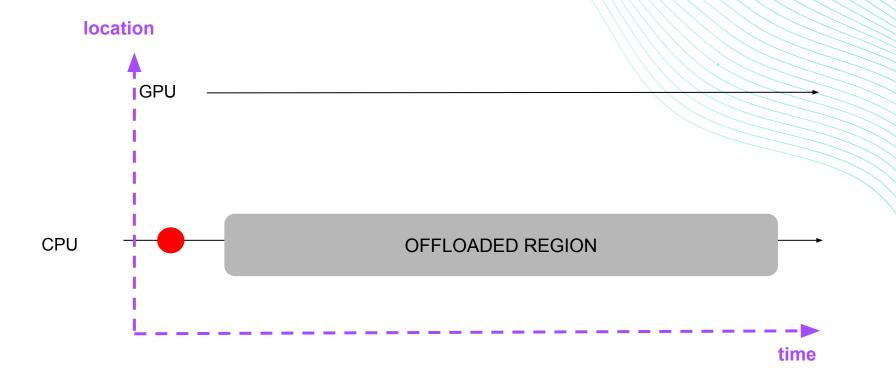
$$D(i) = A * X(i) + Y(i)$$

end do

!\$acc end parallel do

!\$acc parallel do	pgfortran -fast -acc -gpu=cc80,cuda12.3 -Minfo=accel -o binary daxpy.f90
do i = 1, N	daxpy: 19, Generating NVIDIA GPU code 20, !\$acc loop gang, vector(128) ! blockidx%x threadidx%x
D(i) = A* X(i) + Y(i)	19, Generating implicit copyout(y(1:2147483647),x(1:2147483647),d(1:2147483647)) [if not already present]
end do	26, Generating NVIDIA GPU code 27, !\$acc loop gang, vector(128) ! blockidx%x threadidx%x
!\$acc end parallel do	26, Generating implicit copyin(y(1:2147483647),x(1:2147483647)) [if not already present] Generating implicit copyout(d(1:2147483647)) [if not already present]



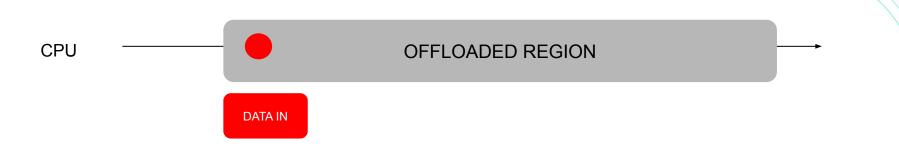


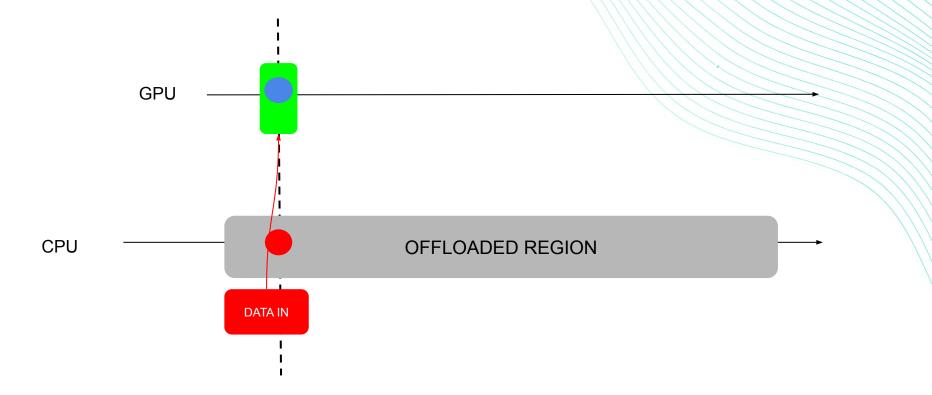
GPU

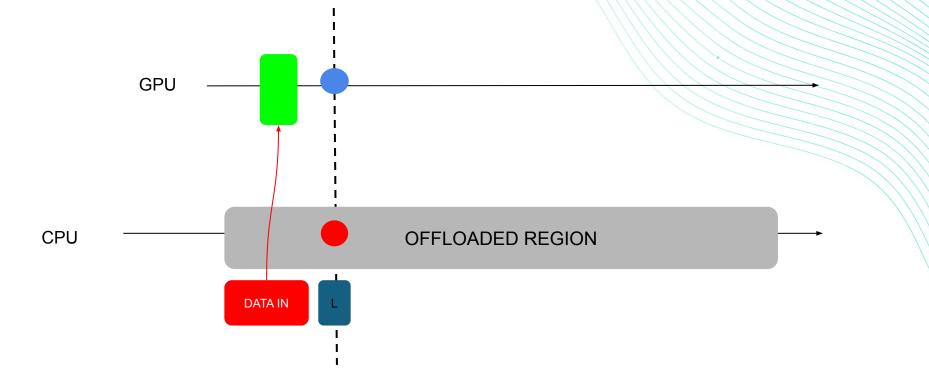
CPU

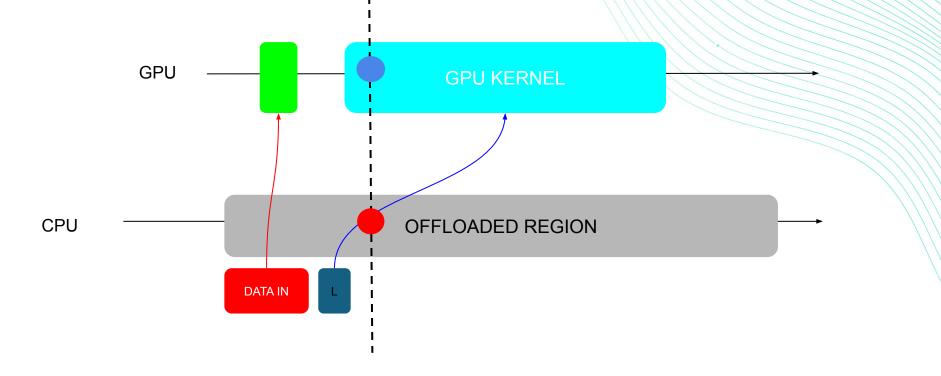
OFFLOADED REGION

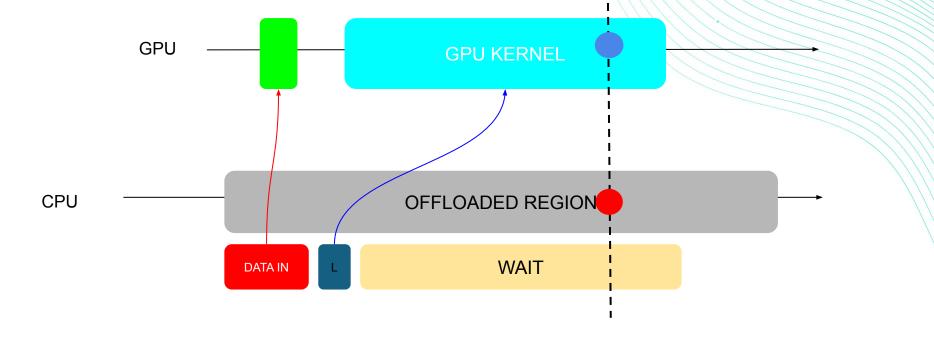
GPU

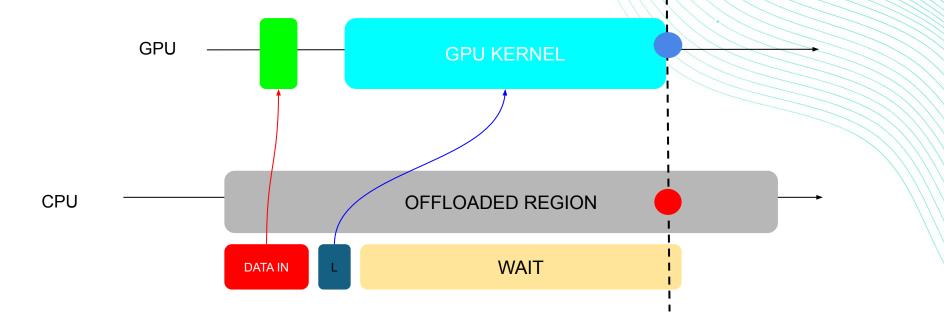


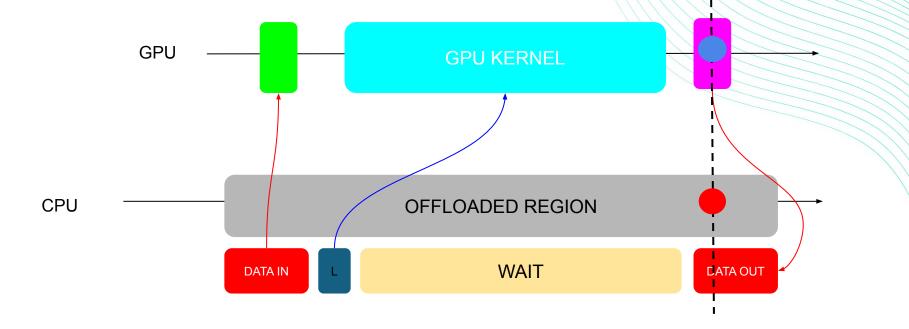


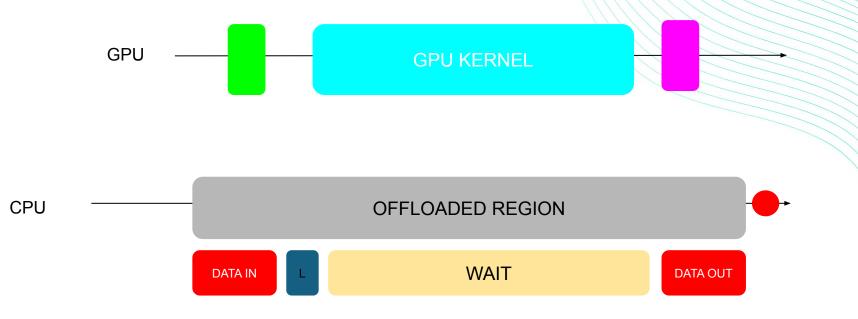












#### **Data clauses**

Data clauses allow the programmer to tell the compiler which data to move and when

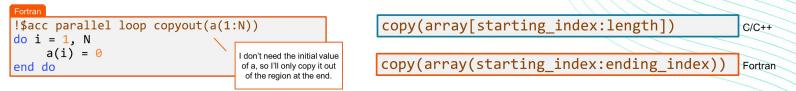


- Fortran programmers can rely on the self-describing nature of Fortran arrays
- C/C++ programmers will frequently need to give additional information to the compiler so that it will know how large an array to allocate on the device and how much data needs to be copied

e.g. copy(array[:]) copy(array[:]) copy(array[:N])

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- Fortran programmers can rely on the self-describing nature of Fortran arrays
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e.g. copy(array[:]) copy(array[:]) copy(array[:N])

array shaping: can move also chunks of arrays (minimize data movements)

#### **Data clauses**

# copy(list)Allocates memory on GPU and copies data from host to GPU when<br/>entering region and copies data to the host when exiting region.Principal use:For many important data structures in your code, this is a<br/>logical default to input, modify and return the data.

#### copyin(list) Allocates memory on GPU and copies data from host to GPU when entering region.

**Principal use:** Think of this like an array that you would use as just an input to a subroutine.

#### copyout ( *list* ) Allocates memory on GPU and copies data to the host when exiting region.

**Principal use:** A result that isn't overwriting the input data structure.

**create**(*list*) Allocates memory on GPU but does not copy.

Principal use: Temporary arrays.

#### Implicit data management

```
while ( error > tol && iter < iter_max )</pre>
  error = 0.0;
  #pragma acc kernels
    for( int j = 1; j < n-1; j++)</pre>
       for( int i = 1; i < m-1; i++ )</pre>
       Anew[j][i] = 0.25 * ( A[j][i+1] + A[j][i-1]+ A[j-1][i] + A[j+1][i]);
       error = fmax( error, fabs(Anew[j][i] - A[j][i]));
    for( int j = 1; j < n-1; j++)
       for( int i = 1; i < m-1; i++ )</pre>
       A[j][i] = Anew[j][i];
```

The runtime automatically handles data movements

For any parallel or kernels construct, it will move data in and out the GPU automatically

This might be very inefficient if the parallel region is inside a loop → data would be moved in/out the GPU for each "kernels"

a, b, c must be visible in the device memory

 $a \rightarrow in$  $b \rightarrow in$  $c \rightarrow out$ 

#pragma acc parallel loop
for(int i = 0; i < N; i++){
 c[i] = a[i] + b[i];
}</pre>

a, b, c must be visible in the device memory

```
#pragma acc data copyin(a[0:N],b[0:N])
copyout(c[0:N])
```

```
#pragma acc parallel loop
for(int i = 0; i < N; i++){
    c[i] = a[i] + b[i];
}</pre>
```

#pragma acc end data

 $a \rightarrow in$   $b \rightarrow in$  $c \rightarrow out$ 

we can explicitly tell the compiler to copyin(a,b) and copyout(c) for a given region of the source code

The acc data directives opens a **data region** 

```
#pragma acc parallel loop
for(int i = 0; i < N; i++){
    a[i] = a[i] + 1.0;
}
#pragma acc parallel loop
for(int i = 0; i < N; i++){
    b[i] = 2.0;
}
#pragma acc parallel loop
for(int i = 0; i < N; i++){
    c[i] = a[i] + b[i];
}</pre>
```

a copied in an out

b copied in and out

a,b copied in and c copied out

```
#pragma acc data copyin(a[0:N],b[0:N])
copyout(c[0:N])
```

```
#pragma acc parallel loop
for(int i = 0; i < N; i++){
    a[i] = a[i] + 1.0;
}
#pragma acc parallel loop
for(int i = 0; i < N; i++){
    b[i] = 2.0;
}
#pragma acc parallel loop
for(int i = 0; i < N; i++){
    c[i] = a[i] + b[i];
}</pre>
```

#pragma acc end data

Inside the data region, the runtime knows a,b,c are in GPU memory

Enclosing parallel/kernels in the same data region reduces the number of data copies

a,b copied in

...gpu work...

c copied out

### Implicit data region

```
#pragma acc parallel loop [copy(a[0:N])]
for(int i = 0; i < N; i++){
        a[i] = a[i] + 1.0;
}</pre>
```

```
#pragma acc data copy(a[0:N]){
    #pragma acc parallel loop
    for(int i = 0; i < N; i++){
        a[i] = a[i] + 1.0;
    }
}</pre>
```

parallel and kernels open an implicit data region

The data region extends for the extension of the parallel/kernel region

#pragma acc enter data copyin(a[0:N],b[0:N])

```
#pragma acc parallel loop
for(int i = 0; i < N; i++){
    a[i] = a[i] + 1.0;
}
#pragma acc parallel loop
for(int i = 0; i < N; i++){
    b[i] = 2.0;
}
#pragma acc parallel loop
for(int i = 0; i < N; i++){
    c[i] = a[i] + b[i];
}</pre>
```

#pragma acc exit data copyout(c[0:N])

enter/exit data are used to create/upload or delete/download data

#### enter data

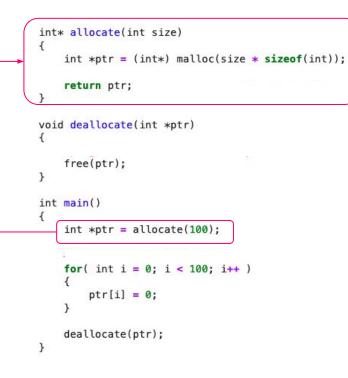
- + create
- + copyin

#### exit data

- + delete
- + copyout

enter/exit data perform only data movement, do not open any data region

Unstructured	Structured		
<ul> <li>Can have multiple starting/ending points</li> </ul>	<ul> <li>Must have explicit start/end points</li> </ul>		
<ul> <li>Can branch across multiple functions</li> </ul>	<ul> <li>Must be within a single function</li> </ul>		
<ul> <li>Memory exists until explicitly deallocated</li> </ul>	<ul> <li>Memory only exists within the data region</li> </ul>		
<pre>#pragma acc enter data copyin(a[0:N],b[0:N]) \</pre>	<pre>#pragma acc data copyin(a[0:N],b[0:N]) \</pre>		
<pre>#pragma acc parallel loop for(int i = 0; i &lt; N; i++){</pre>	<pre>#pragma acc parallel loop for(int i = 0; i &lt; N; i++){</pre>		
<pre>#pragma acc exit data copyout(c[0:N]) \     delete(a,b)</pre>	}		



Data lifetime might not be restricted to a single routine

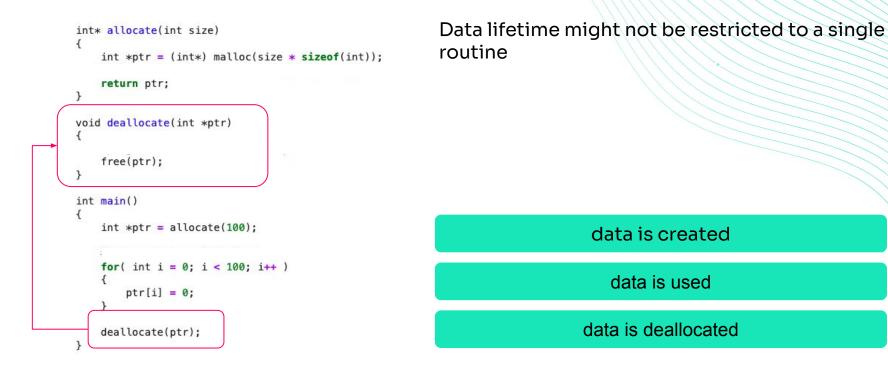
#### data is created

```
int* allocate(int size)
    int *ptr = (int*) malloc(size * sizeof(int));
    return ptr;
}
void deallocate(int *ptr)
    free(ptr);
3
int main()
    int *ptr = allocate(100);
    for( int i = 0; i < 100; i++ )</pre>
        ptr[i] = 0;
    deallocate(ptr);
```

Data lifetime might not be restricted to a single routine

#### data is created

data is used



```
int* allocate(int size)
    int *ptr = (int*) malloc(size * sizeof(int));
    #pragma acc enter data create(ptr[0:size])
    return ptr;
3
void deallocate(int *ptr)
    #pragma acc exit data delete(ptr)
    free(ptr);
int main()
    int *ptr = allocate(100);
    #pragma acc parallel loop
    for( int i = 0; i < 100; i++ )</pre>
        ptr[i] = 0;
    deallocate(ptr);
}
```

Data lifetime might not be restricted to a single routine

#### data is created

data is used

data is deallocated

Be careful when you manage data across multiple routines.

If you try copying data that is already PRESENT on the GPU, the copy is not done.

< a modified on the host >

**#pragma acc enter data copyin(a[0:N])**  $\rightarrow$  host and device copies are in sync

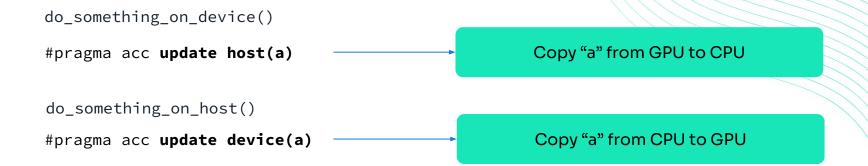
< a modified on the host >  $\rightarrow$  host and device copies are out of sync

#pragma acc data copyin(a[0:N]) ! copy is ignored

< a used on the GPU >  $\rightarrow$  host and device copies are out of sync

## **Update directive**

Data is already on the GPU and you need to update the value on the CPU or device



! The update can also be partial (shaping), e.g. #pragma acc update host(a[0:N/2])

# **Update directive**

**update**: Explicit transfers data between the host and device Useful when you want to synchronise data in the middle of a data region

self / host	makes host data agree with device data
device	makes device data agree with host data

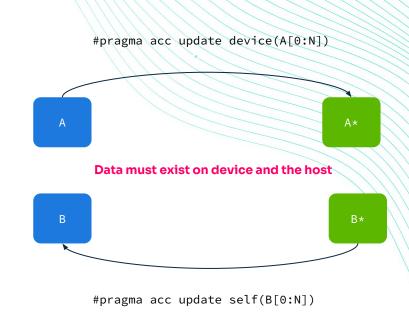
#### C/C++

#pragma acc update self(x[0:count])
#pragma acc update device(x[0:count])

#### Fortran

!\$acc update self(x[1:count])

!\$acc update device(x[1:count])



### **Declare directive**

The declare directive specifies that a variable or array has to be allocated in the device memory for the duration of the implicit data region of function.

- \* Used in the declaration section of function
- \* May specify whether the data have to be transferred and how (create, copy, etc)
- \* If referring to global variables, the implicit region is the whole program



#pragma acc declare create(a[0:N])

Fortran real a(100)

!\$acc declare create(a)























**Gangs** do not share resources, do not synchronize, are independent groups of working units

**Workers** in a gang can share resources, can synch, each one having a roller of a given size (vector length)

A **vector** has the ability to run a single instruction on multiple data elements

```
#pragma acc parallel loop gang
for( i = 0; i < N; i++ )
    #pragma acc loop vector
    for( j = 0; j < M; j++ )
        < loop code >
```

(0, <del>3)</del>	(0,1)	(0,2)	Vec	tor)	(0,5)	(0,6)	<del>(</del> Э,7)	1 Worker Gang
(1,0)	(1,1)	(1,2)	(1,3)	(1,4)	(1,5)	(1,6)	(1,7)	
(2,0)	(2,1)	(2,2)	(2,3)	(2,4)	(2,5)	(2,6)	(2,7)	
(3,0)	(3,1)	(3,2)	(3,3)	(3,4)	(3,5)	(3,6)	(3,7)	

The gang parallelism applies to the outer loop

A vector is the lowest level of parallelism, and every gang will have at least 1 vector

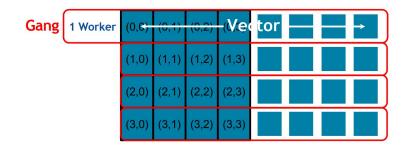
Usually the compiler generates N gangs with one worker and a vector of size 128 on NVIDIA gpus

check with -Minfo!

```
#pragma acc parallel num_workers(2)
#pragma acc loop gang worker
for( i = 0; i < N; i++ )
    #pragma acc loop vector
    for( j = 0; j < M; j++ )
        < loop code >
```

Sometimes having more workers in a gang helps to better map the data

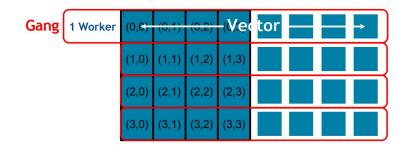
Especially if the size for the vector length is small

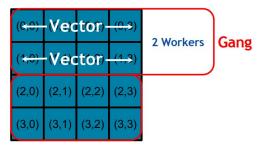


```
#pragma acc parallel num_workers(2)
#pragma acc loop gang worker
for( i = 0; i < N; i++ )
    #pragma acc loop vector
    for( j = 0; j < M; j++ )
        < loop code >
```

Sometimes having more workers in a gang helps to better map the data

Especially if the size for the vector length is small





parallel:

- % num\_gangs(n)
- % num\_workers(n)
- \* vector\_length(n)

#### kernels:

- % gang(n)
- \* worker(n)
- \* vector(n)

The size of a gang is

num\_workers \* vector\_length

the maximum vector\_length is 1024

the minimum vector\_length (NVIDA) is 32

the maximum size of a gang is 1024

### **Routine directive**

**routine** Specifies that the compiler should generate a device copy of the function/subroutine

#### **CLAUSES**

\* gang/worker/vector/seq:

parallelism for loops contained in the routine

\* bind()

optional name of the routine at call-site

\* no\_host

the routine will only be used on the device

void square\_array(float \*arr, int length) {
 for(int i = 0; i < length; ++i) {
 arr[i] = arr[i] \* arr[i];
 }
}</pre>

```
int main() {
   const int size = 100; float data[size];
   #pragma acc parallel loop
   for(int i = 0; i < size; ++i) {
        data[i] = i;
    }
   for(int i = 0; i < size; ++i) {
        square_array(&data[i], 1);
   }
}</pre>
```

### **Routine directive**

**routine** Specifies that the compiler should generate a device copy of the function/subroutine

#### **CLAUSES**

% gang/worker/vector/seq:

parallelism for loops contained in the routine

\* bind()

optional name of the routine at call-site

\* no\_host

the routine will only be used on the device

```
#pragma acc routine worker
void square_array(float *arr, int length) {
    #pragma acc parallel loop worker
    for(int i = 0; i < length; ++i)
        arr[i] = arr[i] * arr[i];
    }
}
int main() {
    const int size = 100; float data[size];
    #pragma acc parallel loop
    for(int i = 0; i < size; ++i) {</pre>
        data[i] = i;
    #pragma acc parallel
        #pragma acc loop gang
        for(int i = 0; i < size; ++i) {</pre>
            square_array(&data[i], 1);
        }
    }
}
```

### **Routine directive**

The **seq** clause in the **routine** directive for OpenACC is used to indicate that the specified routine should be executed **sequentially in one device thread** (GPU).

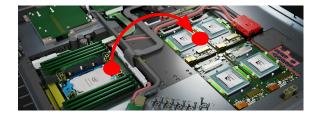
#### At call the compiler needs to know

- \* Function will be available on the GPU (!\$acc routine)
- \* It is a sequential routine, executed by one device thread (seq )

#### At call site

- \* Function is called in a parallel loop region ( parallel loop )
- \* Each thread in the loop will call it and execute its own instance

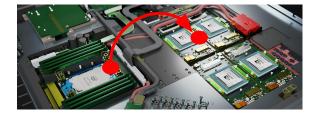
```
module b1
  contains
   real function sqab(a)
      !$acc routine seq
      real :: a
      sqab = sqrt(abs(a))
   end function
  end module
subroutine test( x, n )
     use b1
     real, dimension(*) :: x
     integer :: n
     integer :: i
     !$acc parallel loop copy(x(1:n))
     do i = 1, n
        x(i) = sqab(x(i))
     enddo
  end subroutine
```



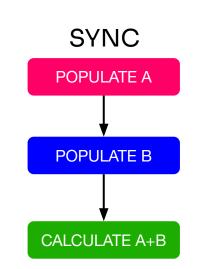
```
for (i = 0; i<n: i++)
a[i] = 1
```

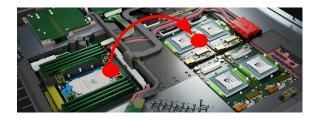
```
for (i = 0; i<n: i++)
b[i] = 1
```

```
for (i = 0; i<n: i++)
c[i] = a[i] + b[i]</pre>
```



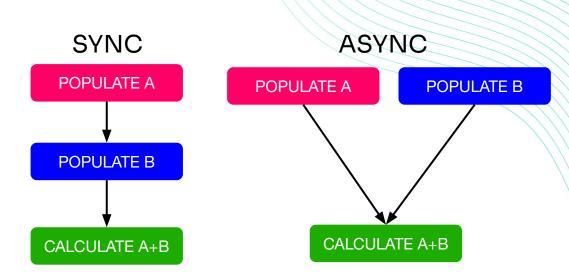
```
for (i = 0; i<n: i++)
a[i] = 1
for (i = 0; i<n: i++)
b[i] = 1
for (i = 0; i<n: i++)
c[i] = a[i] + b[i]</pre>
```





```
for (i = 0; i<n: i++)
a[i] = 1
for (i = 0; i<n: i++)
b[i] = 1
for (i = 0; i<n: i++)</pre>
```

c[i] = a[i] + b[i]



Enables concurrent operations on a GPU

So far all of the OpenACC directives operates synchronously with the host, i.e host will wait for device to complete its execution.

#### async

It can be used on parallel, kernel and update directives

```
#pragma acc loop async
for (i = 0; i<n: i++)
c[i] = a[i] + b[i]</pre>
```



So far all of the OpenACC directives operates synchronously with the host, i.e host will wait for device to complete its execution.

#### async

It can be used on parallel, kernel and update directives

```
#pragma acc loop async
for (i = 0; i<n: i++)
c[i] = a[i] + b[i]
#pragma acc update self[c[0:N]] async</pre>
```



So far all of the OpenACC directives operates synchronously with the host, i.e host will wait for device to complete its execution.

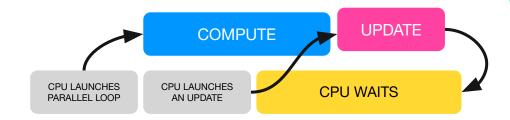
#### async

It can be used on parallel, kernel and update directives

### wait

Instructs the runtime to wait for the past asynchronous operation to complete before proceeding

```
#pragma acc loop async
for (i = 0; i<n: i++)
c[i] = a[i] + b[i]
#pragma acc update self[c[0:N]] async
#pragma acc wait</pre>
```



So far all of the OpenACC directives operates synchronously with the host, i.e host will wait for device to complete its execution.

#### async

It can be used on parallel, kernel and update directives

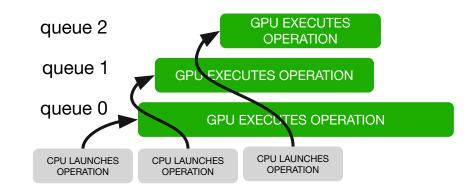
### wait

Instructs the runtime to wait for the past asynchronous operation to complete before proceeding

### async(N)

a number can be added to async and wait, in order to identify the "queue" for the async operation

```
#pragma acc loop async(N)
for (i = 0; i<n: i++)
c[i] = a[i] + b[i]
#pragma acc update self[c[0:N]] async(N)
#pragma acc wait</pre>
```



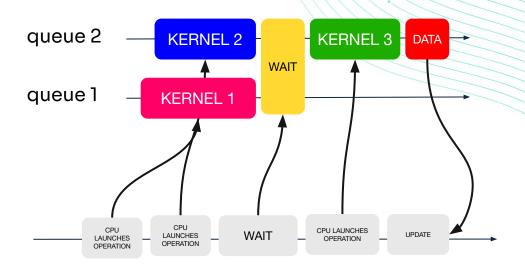
#pragma acc parallel loop async(1)
for (i = 0; i<n: i++)
 a[i] = 1
#pragma acc parallel loop async(2)
for (i = 0; i<n: i++)
 b[i] = 1
#pragma acc wait(1) async(2)
#pragma acc loop async(2)
for (i = 0; i<n: i++)
 c[i] = a[i] + b[i]
#pragma acc update self[c[0:N]] async(2)
#pragma acc wait</pre>

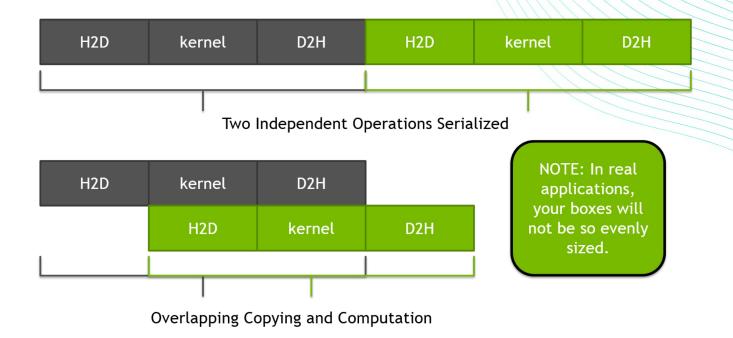
KERNEL 1 IS COMPUTED ON "STREAM" 1

KERNEL 2 IS COMPUTED ON "STREAM" 2

THIS KERNEL WAITS FOR OPERATION IN 1 TO BE COMPLETED AND THEN IS PUT IN THE QUEUE OF STREAM 2

WHEN STREAM2 HAS COMPLETED THE OPERATION, THE HOST IS UPDATED





### **CUDA – OpenACC interoperability**

How to use a CUDA APIs in OpenACC code?

**CUDA** : use device buffer as input/output

ierr = ierr + cufftExecC2C(iplan1,a\_d,b\_d,CUFFT\_FORWARD)

### **CUDA – OpenACC interoperability**

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**OpenACC**: the name of the variable is the the same for device and host buffer. host\_data use\_device directives clarifies which buffer should be passed.

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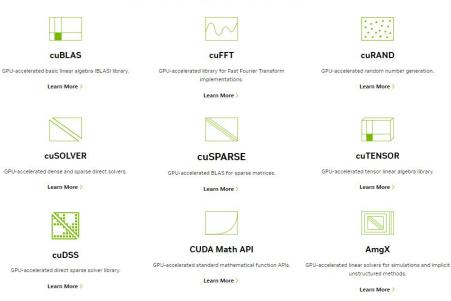
**OpenACC**: the name of the variable is the the same for device and host buffer. host\_data use\_device directives clarifies which buffer should be passed.

```
#pragma acc host_data use_device(a,b)
ierr = ierr + cufftExecC2C(iplan1,a,b,CUFFT_FORWARD)
#pragma acc end host_data
```

### **CUDA** libraries

#### **CUDA Math Libraries**

GPU-accelerated math libraries lay the foundation for compute-intensive applications in areas such as molecular dynamics, computational fluid dynamics, computational chemistry, medical imaging, and seismic exploration.



- \* Offload math to GPU
- Support data moved both with CUDA and OpenACC

Available in the CUDA toolkit or HPCSDK suite, can be linked by compilation flag

Multiple versions available

- \* single gpu (e.g. cuBLAS)
  - batched

\*

- multi-stream
- single-process multi GPU (cuBLASXt)
- \* multi-process multi-GPU (cuBLASMp)

### **CUDA** libraries

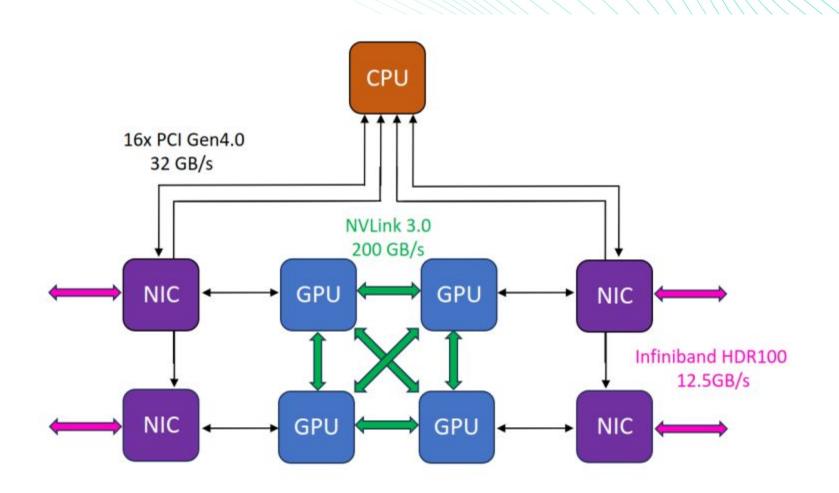
CUDAFortran provides

- \* interfaces to CUDA C library APIs (cuBLAS, cuFFT, cuRANDS, cuSPARSE,...)
- \* interfaces to CPU or GPU API depending on the input type

use cufft use openacc

```
...
!$acc data copyin(a), copyout(b,c)
ierr = cufftPlan2D(iplan1,m,n,CUFFT_C2C)
ierr = ierr +
cufftSetStream(iplan1,acc_get_cuda_stream(acc_async_sync))
!$acc host_data use_device(a,b,c)
ierr = ierr + cufftExecC2C(iplan1,a,b,CUFFT_FORWARD)
ierr = ierr + cufftExecC2C(iplan1,b,c,CUFFT_INVERSE)
!$acc end host_data
```

!\$acc kernels
c = c / (m\*n)
!\$acc end kernels
!\$acc end data





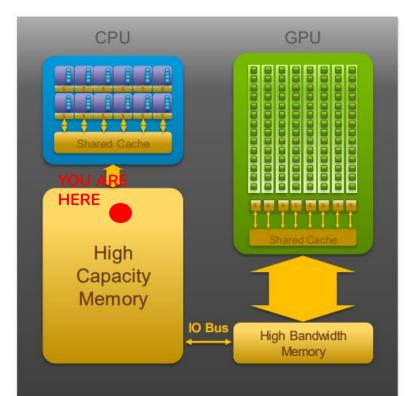
# **Profiling with NSight Systems**

Epicure hackathon @ CINECA, Casalecchio di Reno (BO) Italy 28-31 October 2024

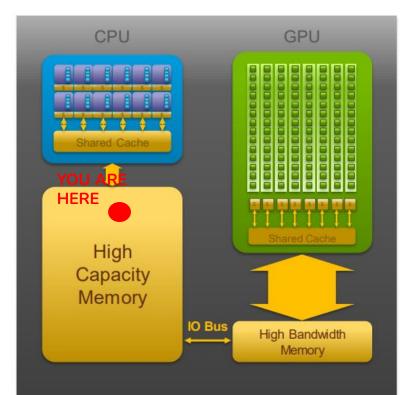




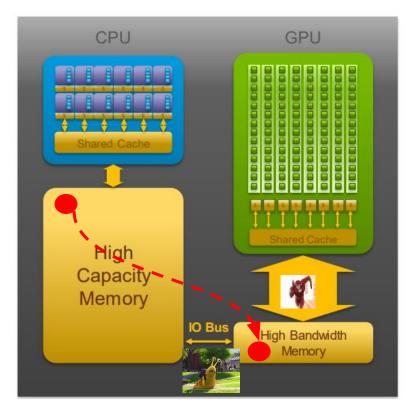
This project has received funding from the High Performance Computing Joint Undertaking under grant agreement No 101139786



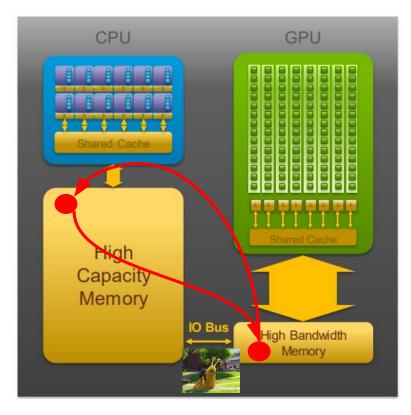
The program starts on the CPU



- The program starts on the CPU
- GPUs and CPUs have separated memories

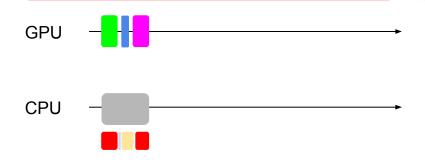


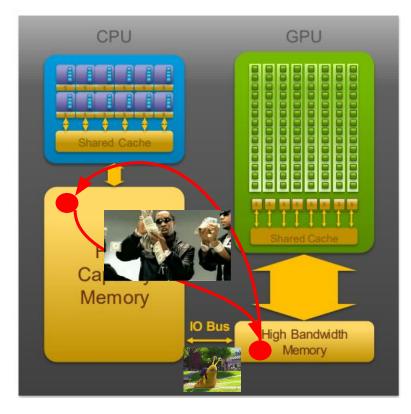
- The program starts on the CPU
- GPUs and CPUs have separated memories
- GPUs need data in their own memory



- The program starts on the CPU
- GPUs and CPUs have separated memories
- GPUs need data in their own memory
- IO bus is slow compared to GPU BW

### MOVING DATA IS EXPENSIVE

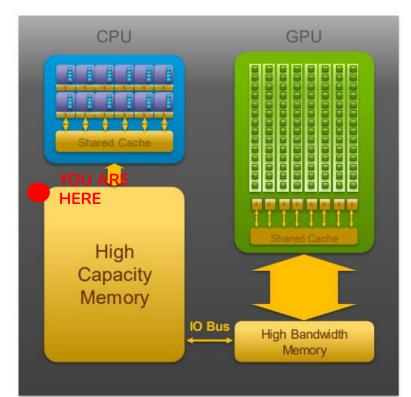




- The program starts on the CPU
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### MOVING DATA IS EXPENSIVE

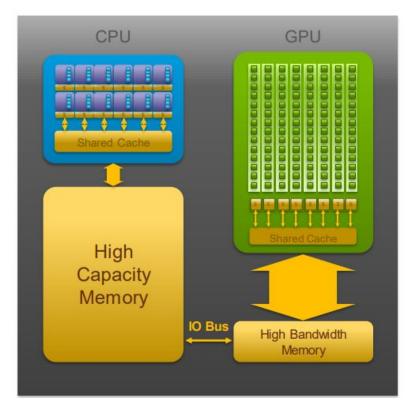




- The program starts on the CPU
- GPUs and CPUs have separated memories
- GPUs need data in their own memory
- IO bus is slow compared to GPU BW

### MOVING DATA IS EXPENSIVE

### IMPROVE DATA LOCALITY

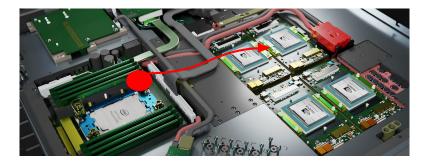


- The program starts on the CPU
- GPUs and CPUs have separated memories
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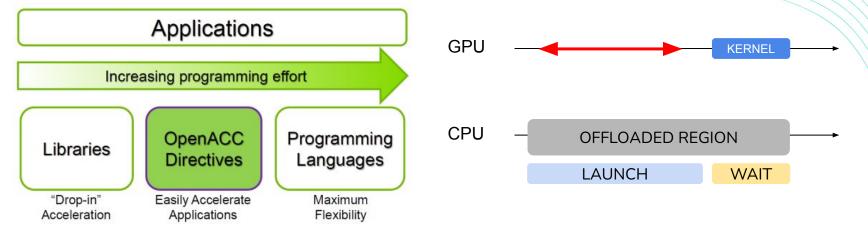
### MOVING DATA IS EXPENSIVE

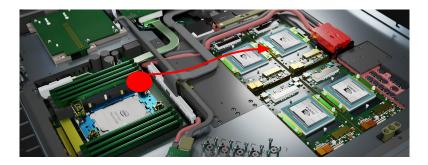


CPU

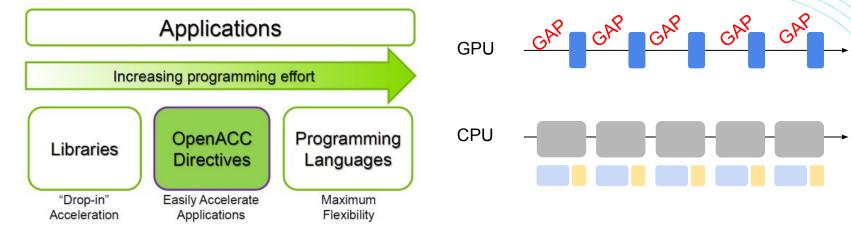


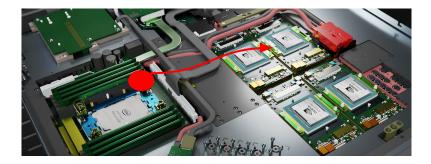
- The program starts on the CPU
- Many ways to offload kernels to GPUs
- There is a time needed to launch the kernels ("latency")

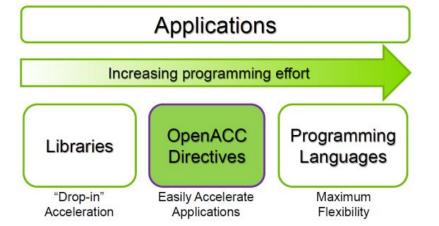




- The program starts on the CPU
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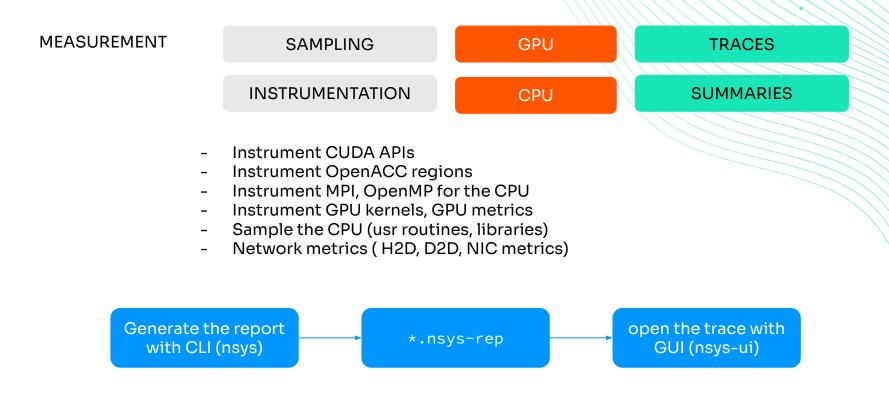
- The program starts on the CPU
- Many ways to offload kernels to GPUs
- There is a time needed to launch the kernels ("latency")

### AVOID SMALL KERNELS

### EXPOSE AS MUCH PARALLELISM AS POSSIBLE

### COLLAPSE LOOPS, REFACTOR

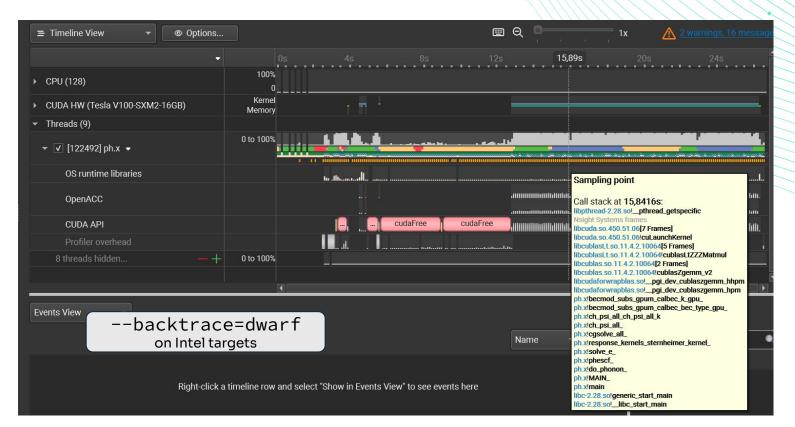
# **NSight Systems**



## **Timeline view**

	🚍 Q 🕛	1x A 2 warnings, 16 message
19s <b>-</b>	s +793ms +794ms +795ms +796ms	+797ms +798ms +799ms +800
	100%	cpu activity
CPU 2	0 to 100%	
CPU 3	0 to 100%	
CPU 1	0 to 100% [122492] ph.x	
CPU 0	0 to 100%	gpu kernels
✓ CUDA HW (Tesla V100-SXM2-16GB)	Kernel Memory	بر - مردم در روب ها مدر روب مردمه ا
▶ 78,1% Kernels	nan <mark>nanta a statuta anana tahi a antita alahanah aa ataana.</mark> at	atala a mi cara ta cara ta ta cara ta ta cara ta ta cara ta car
▶ 21,9% Memory	and the second second second	
✓ Threads (9)		
▼ ✔ [122492] ph.x 🔹	0 to 100%	data movements
OS runtime libraries		
OS runtime libraries	a National and a state of a state of the state	
OpenACC	i i indiato interna i i indiato di i i indiato interna i i indiato da indiato indiato indiato indiato indiato i Attili indiato i	i i u ununuta antami i u antikata utani i u antika Attikati kanta inalikati attaat attaat
CUDA API	liden and a submit the second statistic terms of the second statistic statistic statistic statistic statistics	Add home is him for the full domain a month is to the line bound of
Profiler overhead		library instrumentation
8 threads hidden+	0 to 100% CUDA backend	

# **CPU** sampling



### **Summaries**

Flat View	▼ Na	tive 🔻	Process [122492] ph.x (9 of 9 threads)				
Filter 49.703 samples are used.							
Symbol Name 🛛 Self, % 🛛 Stack, % 🔻 Module Name							
libc_start		74,08	/usr/lib64/power9/libc-2.28.so				
generic_star	•	74,08	/usr/lib64/power9/libc-2.28.so				
main		74,03	/m100_scratch/userinternal/lbellen1/qe_src/prototipo0/gpuv/build_nonvtx/bin/ph.x				
MAIN_	•	74,03	/m100_scratch/userinternal/lbellen1/qe_src/prototipo0/gpuv/build_nonvtx/bin/ph.x				
do_phonon_		65,88	/m100_scratch/userinternal/lbellen1/qe_src/prototipo0/gpuv/build_nonvtx/bin/ph.x				
cgsolve_all_	0,01	50,25	/m100_scratch/userinternal/lbellen1/qe_src/prototipo0/gpuv/build_nonvtx/bin/ph.x				
ch_psi_all_	0,03	49,41	/m100_scratch/userinternal/lbellen1/qe_src/prototipo0/gpuv/build_nonvtx/bin/ph.x				
response_ke	0,01	45,22	/m100_scratch/userinternal/lbellen1/qe_src/prototipo0/gpuv/build_nonvtx/bin/ph.x				
phqscf_		36,51	/m100_scratch/userinternal/lbellen1/qe_src/prototipo0/gpuv/build_nonvtx/bin/ph.x				
solve_linter_	•	3 <mark>6,37</mark>	/m100_scratch/userinternal/lbellen1/qe_src/prototipo0/gpuv/build_nonvtx/bin/ph.x				
phescf_	•	29 <mark>.01</mark>	01 /m100_scratch/userinternal/lbellen1/qe_src/prototipo0/gpuv/build_nonvtx/bin/ph.x				
solve_e_	•2	28 <mark>,42</mark>	/m100_scratch/userinternal/lbellen1/qe_src/prototipo0/gpuv/build_nonvtx/bin/ph.x				
clone	<b>1</b> 0	25, <mark>44</mark>	/usr/lib64/power9/libc-2.28.so				
start_thread	•	25, <mark>44</mark>	/usr/lib64/power9/libpthread-2.28.so				
h_psi_gpu_	•	23, <mark>88</mark>	/m100_scratch/userinternal/lbellen1/qe_src/prototipo0/gpuv/build_nonvtx/bin/ph.x				
h_psigpu_	0,01	23, <mark>05</mark>	/m100_scratch/userinternal/lbellen1/qe_src/prototipo0/gpuv/build_nonvtx/bin/ph.x				
0v2000585f	0.10	18 58	/usr/lib64/libcuda so 450 51 06				

### **Statistics**

Stats Syster	n View 👻							
Fime 🝷	Total Time	Instances	Avg	Med	Min	Max	StdDev	Name
19.0%	137,204 ms	42020	3,265 µs	3,355 µs	2,843 µs	6,621 µs	329 ns	void composite_2way_fft<20u, 4u, 32u, (padding_t)0, (twic
18.0%	130,783 ms	22556	5,798 µs	5,756 µs	5,499 µs	14,618 µs	292 ns	volta_zgemm_32x32_nn
17.0%	123,229 ms	16917	7,284 µs	7,356 µs	6,045 µs	12,861 µs	374 ns	void zgemm_largek_warp <true, 3,="" 3,<="" 4,="" false,="" td="" true,=""></true,>
10.0%	71,216 ms	21010	3,389 µs	3,453 µs	2,810 µs	6,972 µs	457 ns	void composite_2way_fft<20u, 4u, 16u, (padding_t)0, (twic
2.0%	19,550 ms	8285	2,359 µs	2,748 µs	1,435 µs	3,357 µs	559 ns	fft_scalar_cufft_cfft3d_gpu_586_gpu
2.0%	18,334 ms	12010	1,526 µs	1,531 µs	1,499 µs	2,109 µs	17 ns	add_vuspsi_k_gpu_248_gpu
2.0%	17,736 ms	16917	1,048 µs	1,052 µs	986 ns	1,468 µs	23 ns	void scal_kernel <double2, 1,="" 4="" 4,="" 5,="" double2,="" true,="">(cubl</double2,>
2.0%	17,436 ms	12010	1,451 µs	1,438 µs	1,275 µs	1,980 µs	52 ns	dp_dev_memcpy_c2d_770_gpu
2.0%	15,034 ms	6005	2,503 µs	2,590 µs	1,466 µs	3,037 µs	285 ns	vloc_psi_k_gpu_464_gpu
2.0%	14,024 ms	6005	2,335 µs	2,363 µs	2,042 µs	3,644 µs	91 ns	vloc_psi_k_gpu_456_gpu
1.0%	13,388 ms	6005	2,229 µs	2,236 µs	2,013 µs	3,003 µs	57 ns	vloc_psi_k_gpu_477_gpu
1.0%	10,685 ms	6005	1,779 µs	1,787 µs	1,627 µs	3,004 µs	49 ns	h_psigpu_158_gpu
1.0%	9,865 ms	6005	1,642 µs	1,658 µs	1,531 µs	2,237 µs	33 ns	ch_psi_all_132_gpu
1.0%	9,763 ms	6005	1,625 µs	1,628 µs	1,531 µs	2,172 µs	30 ns	ch_psi_all_k_266_gpu

# CLI: nsys command

nsys [command\_switch] [optional command\_switch\_options][application] [optional application\_options

### Command switches

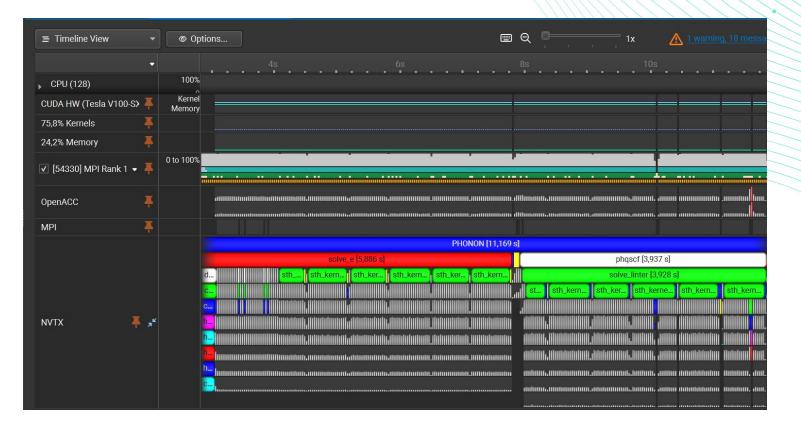
- profile
- start launch cancel shutdown stop
- export stats analyze

#### Command switch options

- All-in-one , needed for concurrent profiling sessions Interactive mode Postprocessing to export / textual summaries
- --trace=[nvtx,cuda,osrt],mpi,openmp,openacc,cublas,cusolver,... Events to trace
- --cuda-memory-usage
- --nic-metrics

Collect GPU memory usage Network bandwidth

Example: nsys profile --trace=openacc,cuda,nvtx cfd.exe > report1.nsys-rep



report1_nonvtx_siph.qdrep X report1ok.qc	lrep (report1.qdrep) ×		
	ptions	■ Q <b>□</b>	1x <u>1 warning, 18 messag</u>
6s <del>•</del>	+153,8ms +154ms +154,2ms	+154,4ms	+154,6ms +154,8ms
CPU (128)			+
CUDA HW (Tesla V100-S 📮 Kernel Memory	e and a second of the constant	i ali nuria	
75,8% Kernels 📕	, and a shall be the statement		
24,2% Memory 📮		ւ վու լ	
<ul> <li>✓ [54330] MPI Rank 1 - </li> </ul>			
OpenACC -			
MPI			
		PHONON [11,169 s] solve_e [5,886 s]	
	stt	kernel [673,537 ms]	
		gsolve [17,172 ms]	
		ch_psi [1,415 ms]	
NVTX 📮 💉			ast [640,174 µs]
	h_psi [544,769 μs] h_psi:pot [492,863 μs]	Hesh [89,	ch_psi_all_k [492,319 µs] ch_psi_c s_p
	vloc_psi [241,168 µs] h_psi:calb add_vuspsi [1		calbe
	fftw [6 fftw [73, Calbe		

NVTX library (nvToolsExt.h) can be used to enhance trace readability:

- C-based API to annotate events and code ranges, to be visualized in the Nsight System timeline
- Limited overhead when the tool is not attached to the application

### **Functionalities**

- NVTX Markers → annotate events occurring at a specific time
- **NVTX Ranges**  $\rightarrow$  annotate timespan of code regions

#### **Events**

- associated to message (ASCII, Unicode)  $\rightarrow$  A, W variant of function calls
- associated to structure with attributes  $\rightarrow$  **Ex** variant of function calls

//Set to default

nvtxEventAttributes\_t eventAttrib {0};

//Declare version and size

eventAttrib.version = NVTX\_VERSION; eventAttrib.size = NVTX\_EVENT\_ATTRIB\_STRUCT\_SIZE;

// Message type and message
// // ASCII

eventAttrib.messageType = NVTX\_MESSAGE\_TYPE\_ASCIT; eventAttrib.message.ascii = \_\_FUNCTION\_\_ ":ascii"; // //UNICODE

eventAttrib2.messageType = NVTX\_MESSAGE\_TYPE\_UNICODE; eventAttrib2.message.unicode = \_\_FUNCTIONW\_\_ L ":unicode \u2603 snowman";

// Color type and color

eventAttrib.colorType = NVTX\_COLOR\_ARGB; eventAttrib.color = COLOR\_YELLOW;

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// Color type and color

eventAttrib.colorType = NVTX\_COLOR\_ARGB; eventAttrib.color = COLOR\_YELLOW;

## **NVTX ranges**

Markers (events at a specific time)

nvtxMarkA(\_\_FUNCTION\_\_ ":nvtxMarkA"); nvtxMarkW(\_\_FUNCTIONW\_\_ L":nvtxMarkW"); nvtxMarkEx(&eventAttrib);

Ranges (nested time ranges occurring on a CPU thread)

start: nvtxRangePushEx

nvtxRangePushA

nvtxRangePushW

end : nvtxRangePop

// for message-only events

nvtxRangePushA(\_\_FUNCTION\_\_ ":nvtxRangePushA");
[... code here ...]
nvtxRangePop();

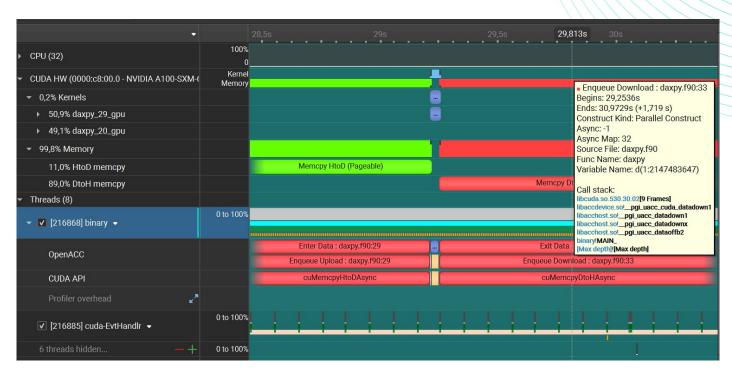
nvtxRangePushW(\_\_FUNCTIONW\_\_ L":nvtxRangePushW"); [... code here ...] nvtxRangePop();

// for structured events

nvtxRangePushEx(&eventAttrib); [... code here ...] nvtxRangePop();

CUDAFortran: interfaces provided by nvtx module ( subroutines nvtxStartRange, nvtxEndRange)

### **DAXPY** profiled



#### **DAXPY** profiled

```
call nvtxstartRange("initialize",1)
!$acc parallel loop
do i = 1, N
    D(i) = 0
    X(i) = 1
    Y(i) = 2
end do
call nvtxEndRange()
call nvtxStartRange("daxpy",2)
!$acc parallel loop
do i = 1, N
    D(i) = A* X(i) + Y(i)
end do
call nvtxEndRange()
```

#### Data movements

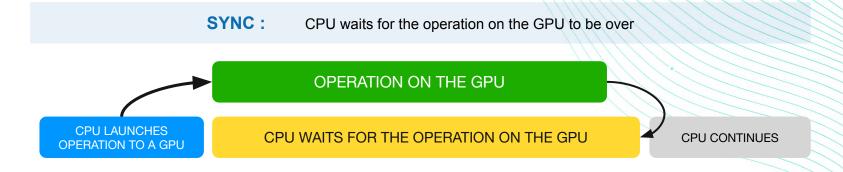
	ions			Q 0	<u>1</u> x
		s	10s	20s	30s
0,2% Kernels	Ŧ				
50,9% daxpy_29_gpu	Ŧ				
49,1% daxpy_20_gpu	Ŧ				
99,8% Memory	<b></b>				
10,9% HtoD memcpy	4				Me Me
89,1% DtoH memcpy	<b>Ļ</b>	Memcpy DtoH (Pageable)	Memcpy DtoH (Pageable)	Memcpy DtoH (Pageable)	Me
✓ [2472332] binary +	0 to 100%				• • • • •
	_		Exit Data : daxpy.f90:20		Enter Da Exit
OpenACC	<b>^</b>	Enqueue Download : daxp Ei	nqueue Download : daxpy.f90	Enqueue Download : daxp	En En En
NVTX	7		initialize [25,346 s]		daxpy [4,996 s]
CUDA API	Ŧ	cuMemcpyDtoHAsync	cuMemcpyDtoHAsync	cuMemcpyDtoHAsync	cu cu cu

#### **GPU** kernels

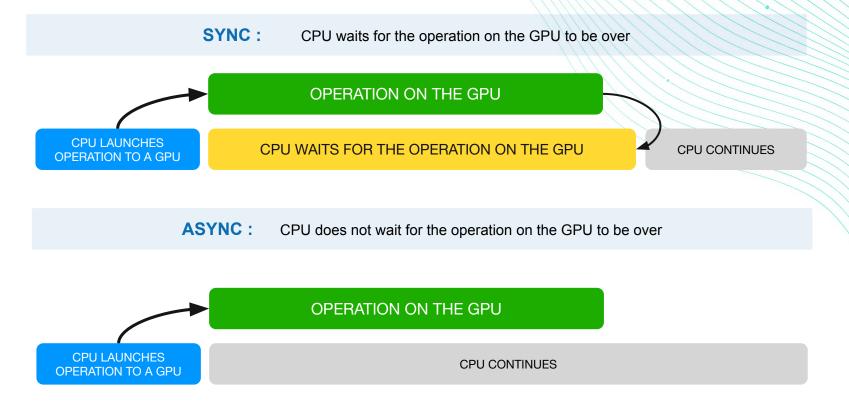
		<u>ଲ</u> ବ୍	1x (1) 15 messa
29s 🗸		+220ms +230ms +240i <b>29s 2</b>	243,40ms +250ms +260ms
► CPU (32)	100% 0		
- CUDA HW (0000:c8:00.0 - NVIDIA A100-SXM-6	Kernel Memory		
👻 0,2% Kernels		daxpy_29_gpu	
▶ 50,9% daxpy_29_gpu		daxpy_29_gpu	
▶ 49,1% daxpy_20_gpu			daxpy_29_gpu Begins: 29,2178s
			Ends: 29,2536s (+35,828 ms) grid: <<<16777216, 1, 1>>>
11,0% HtoD memcpy		Memc	block: <<<128, 1, 1>>>
89,0% DtoH memcpy			Launch Type: Regular Static Shared Memory: 0 bytes (Pagea.
			Dynamic Shared Memory: 0 bytes Registers Per Thread: 18
▼ ✔ [216868] binary 👻	0 to 100%		Local Memory Per Thread: 0 bytes Local Memory Total: 146.276.352 bytes
		Enter Compute Construct : daxpy.f90:29	Shared Memory executed: 32.768 bytes Shared Memory Bank Size: 4 B
OpenACC		Enque Wait : daxpy.f90:29	Theoretical occupancy: 100 % Launched from thread: 216868
CUDA API		cuMe	Latency: ←18,617 µs pHAsync
Profiler overhead			Correlation ID: 41 Stream: Stream 13
✓ [216885] cuda-EvtHandlr	0 to 100%		
6 threads hidden — +	0 to 100%		
	Î		

		🗐 Q 🗖 1x 🚯	15 mess
29s <b>•</b>		+217; 29s 217,7634ms +217,8ms +217,85m	
► CPU (32)	100% 0		
▼ CUDA HW (0000:c8:00.0 - NVIDIA A100-SXM-(	Kernel Memory		
✓ 0,2% Kernels		daxpy_29_gpu	
▶ 50,9% daxpy_29_gpu		daxpy_29_gpu	-
▶ 49,1% daxpy_20_gpu			
11,0% HtoD memcpy	Memcpy HtoD (Pageable)		
89,0% DtoH memcpy			
→ Threads (8)			
	0 to 100%		
OpenACC	Enter Data : daxpy.f90:29 Wait : daxpy.f90:29	Compute Construct : daxpy.f90:29 Enqueue Launch : daxpy Wait : daxpy.f90:29	
CUDA API	cuStreamSynchroni	daxpy_29_g. Engueue Launch : daxpy.f90:29	
Profiler overhead		Begins: 29,2177s Ends: 29,2178s (+34,495 μs)	
✓ [216885] cuda-EvtHandlr 🔸	0 to 100%	Construct Kind: Parallel Construct Async: -1 Async Map: 32	
6 threads hidden — +	0 to 100%	Source File: daxpy.f90 Func Name: daxpy	
		Number of Gangs: 16.777.216	
		Number of Workers: 1 Vector Length: 128 Kernel Name: daxpy_29_gpu	

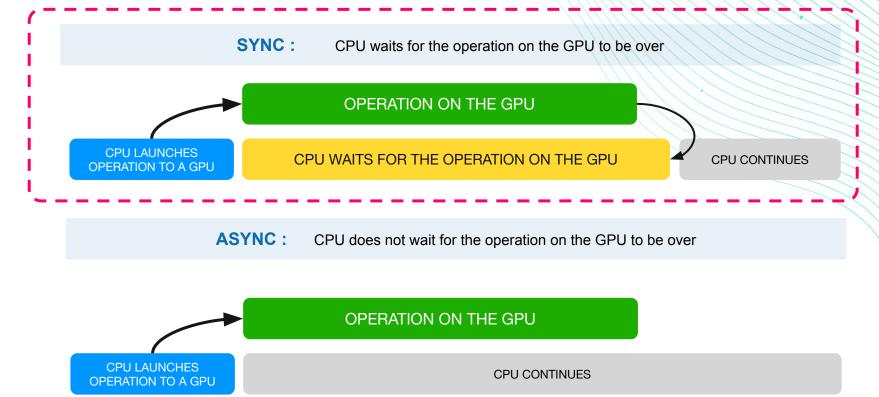
#### Patterns in OpenACC traces



### Patterns in OpenACC traces



#### Patterns in OpenACC traces



#### Patterns for compute directives

By default, OpenACC queues operation on the default stream

Data directives, parallel and kernels impose sync between CPU and GPU

Parallel and kernels embody an implicit data region

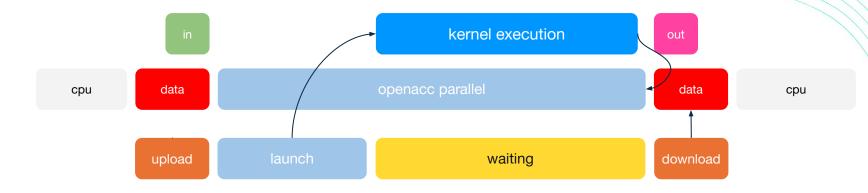
```
!$acc parallel loop [copyout(a)]
do i = 1, N
   a(i) = 0
end do
```

#### Patterns for compute directives

By default, OpenACC queues operation on the default stream

Data directives, parallel and kernels impose sync between CPU and GPU

Parallel and kernels embody an implicit data region



What if parallel/kernels is in a data region?

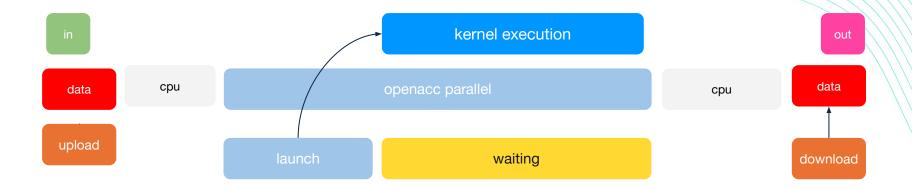
If parallel/kernel is in the same routine of the **structured data region**, the runtime knows that the data is already on the GPU

Remind that enter data does not open a data region!

```
subroutine myloop()
<...>
!$acc data copyout(a)
!$acc parallel loop
do i = 1, N
    a(i) = 0
end do
!$acc end data
<...>
end subroutine
```

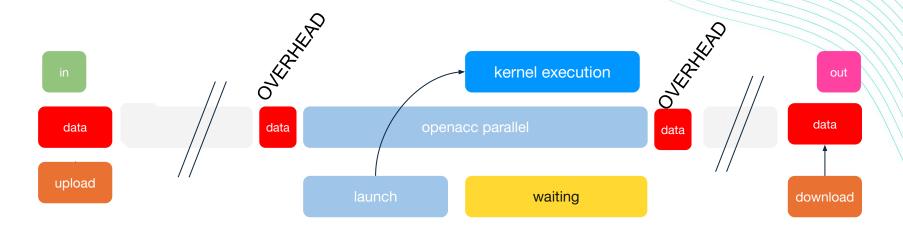
Unless needed to copy some missing variables, the implicit data region is not opened (because already opened!)

If the compute region is in the same routine of the data region, the runtime will not check for variables on the GPU



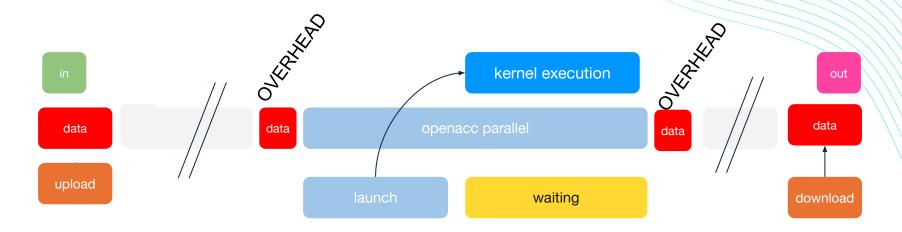
If the compute directive is not in the same routine of the data region, the runtime will check anyways if the data is on the GPU or not

This extra check does not trigger an actual data movement, but it is an overhead

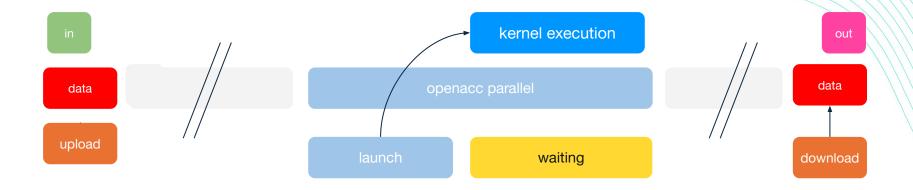


This extra check does not trigger an actual data movement, but it is an overhead

Be careful when using **PRESENT** clause, it forces this extra check, might add an overhead

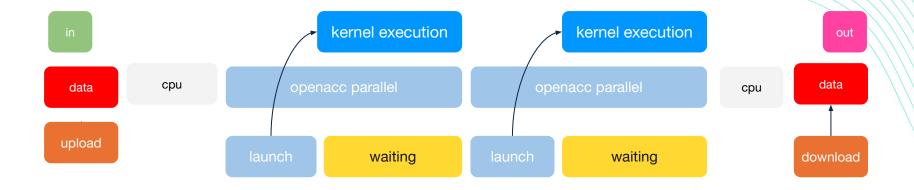


This extra check can be avoided only with the declare directive on a global variables



Unless needed to copy some missing variables, the implicit data region is not opened (because already opened!)

We can open a single data region for multiple kernels



What if a single parallel encloses multiple loops

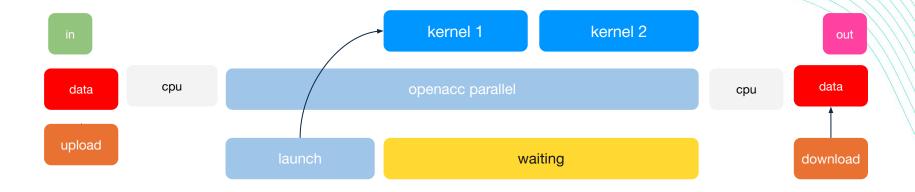
```
!$acc data copyout(a,b)
!$acc parallel
```

```
!$acc loop
do i = 1, N
  a(i) = 0
end do
!$acc loop
do i = 1, N
  b(i) = 0
end do
```

!\$acc end parallel
!\$acc end data

There will be one OpenACC compute region, one single launch and multiple kernels

Avoids multiple kernel launches (reduces overhead)

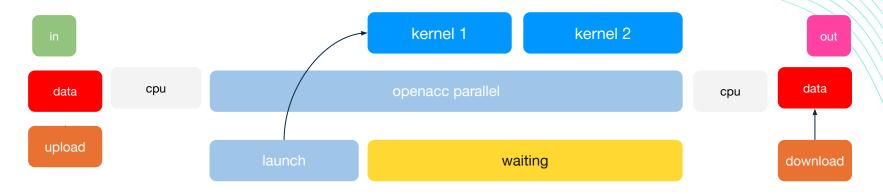


There will be one OpenACC compute region, one single launch and multiple kernels

Avoids multiple kernel launches (reduces overhead)

**! Parallel**: Gangs do not sync: if one gang has finished relative job in kernel 1, continues in kernel 2

! Kernels: imposes a sync barrier



#### Parallel vs kernels

Careful if gangs access different data locations in loops

!\$acc parallel !\$acc loop do i = 1, N D(i) = 0 X(i) = 1 Y(i) = 2 end do !\$acc loop do i = 1, N D(i) = A\*X(i)+Y(i) end do

!\$acc end parallel

```
!$acc parallel
!$acc loop
do i = 1, N
        D(i) = 0
        X(i) = 1
        Y(i) = 2
end do
```

```
!$acc loop
do i = 1, N-1
    D(i) = A*X(i+1)+Y(i+1)
end do
!$acc end parallel
```

!\$acc kernels
do i = 1, N
 D(i) = 0
 X(i) = 1
 Y(i) = 2
end do

#### [implicit wait]

```
do i = 1, N-1
        D(i) = A*X(i+1)+Y(i+1)
end do
!$acc end kernels
```

# Kernels or parallel?

#### Kernels

- Compiler decides what to parallelize with direction from user
- Compiler guarantees correctness
- Can cover multiple loop nests

 Programmer decides what to parallelize and communicates that to the compiler

Parallel

- Programmer guarantees correctness
- Must decorate each loop nest

When fully optimized, both will give similar performance.

#### **Summaries**

nsys stats report1.nsys-rep

Time	🔻 Tota	al Time	Count	Avg N	Med M	Min	Max	StdDev	Operation
	89.0%	27,115 s	4	6,779 s	8,122 s	1,719 s	9,152	s 3,410	s [CUDA memcpy Device-to-Host]
	11.0%	3,359 s	2	1,680 s	1,680 s	1,677 s	1,682	s 3,730 m	s [CUDA memcpy Host-to-Device]
·									
Total	-	Count	Avg	Med	Min	Max		StdDev	Operation
Total	<b>~</b> 64,00 GiB	Count 4	Avg 16,00 Gi			Max 00 GiB	16,00 GiB	StdDev 0 B	Operation [CUDA memcpy Device-to-Host]

Tir	ne 🔻	Total Time	Instances	Avg	Med	Min	Max	StdDev	Category	Operation
	88.0%	27,115 s	4	6,779 s	8,122 s	1,719 s	9,152 s	3,410 s	MEMORY_OPER	[CUDA memcpy Device-to-Host]
	11.0%	3,359 s	2	1,680 s	1,680 s	1,677 s	1,682 s	3,730 ms	MEMORY_OPER	[CUDA memcpy Host-to-Device]
	0.0%	35,828 ms	1	35,828 ms	35,828 ms	35,828 ms	35,828 ms	0 ns	CUDA_KERNEL	daxpy_29_gpu
	0.0%	34,609 ms	1	34,609 ms	34,609 ms	34,609 ms	34,609 ms	0 ns	CUDA_KERNEL	daxpy_20_gpu

#### **OpenACC** runtime

0.0%

0 ns

≡ Tin	neline View		© Options				e e		1x 1 warning, 17	
Stats S	system Viev	v –								
Time	<b>-</b> 1	otal Time	Num Calls	Avg	Med	Min	Max	StdDev	Name	
	41.0%	24,963 s		1 24,963	s 24,963 s	24,963 s	24,963 s	0 ns	Exit Data@daxpy.f90:20	
	41.0%	24,963 s		3 8,321	s 8,041 s	7,832 s	9,091 s	674,577 ms	Enqueue Download@daxpy.f90:2	26
	5.0%	3,250 s		1 3,250	s 3,250 s	3,250 s	3,250 s	0 ns	Enter Data@daxpy.f90:29	
	5.0%	3,250 s		2 1,625	is 1,625 s	1,624 s	1,626 s	2,050 ms	Enqueue Upload@daxpy.f90:29	
	2.0%	1,710 s		1 1,710	ls 1,710 s	1,710 s	1,710 s	0 ns	Exit Data@daxpy.f90:29	
	2.0%	1,710 s		1 1,710	ls 1,710 s	1,710 s	1,710 s	0 ns	Enqueue Download@daxpy.f90:3	33
	0.0%	37,751 ms		1 37,751 n	ns 37,751 ms	37,751 ms	37,751 ms	0 ns	Enter Data@daxpy.f90:20	
	0.0%	35,878 ms		1 35,878 n	ns 35,878 ms	35,878 ms	35,878 ms	0 ns	Compute Construct@daxpy.f90:2	29
	0.0%	35,872 ms		2 17,936 n	ns 17,936 ms	31,261 µs	35,840 ms	25,321 ms	Wait@daxpy.f90:29	
	0.0%	34,669 ms		1 34,669 n	ns 34,669 ms	34,669 ms	34,669 ms	0 ns	Compute Construct@daxpy.f90:2	20
	0.0%	34,635 ms		2 17,317 n	ns 17,317 ms	11,136 µs	34,623 ms	24,475 ms	Wait@daxpy.f90:20	
	0.0%	103,849 µs		1 103,849	us 103,849 µs	103,849 µs	103,849 µs	0 ns	Device Init@daxpy.f90:20	
	0.0%	35,866 µs		1 35,866	us 35,866 µs	35,866 µs	35,866 µs	0 ns	Enqueue Launch@daxpy.f90:20	
	0.0%	33,241 µs		1 33,241	us 33,241 µs	33,241 µs	33,241 µs	0 ns	Enqueue Launch@daxpy.f90:29	
	0.0%	5,756 µs		1 5,756	us 5,756 µs	5,756 µs	5,756 µs	0 ns	Wait@daxpy.f90:26	
	0.0%	4,749 µs		1 4,749	us 4,749 µs	4,749 µs	4,749 µs	0 ns	Wait@daxpy.f90:33	
	0.0%	0 ns		3 01	ns Oins	0 ns	0 ns	0 ns	Alloc@daxpy.f90:20	
	0.0%	0 ns		3 0 1	ns Oins	0 ns	0 ns	0 ns	Create@daxpy.f90:20	
	0.0%	0 ns		3 0 1	ns Oins	0 ns	0 ns	0 ns	Create@daxpy.f90:29	
	0.0%	0 ns		3 0 1	ns Oins	0 ns	0 ns	0 ns	Delete@daxpy.f90:26	

 $0 \, \mathrm{ns}$ 

0 ns

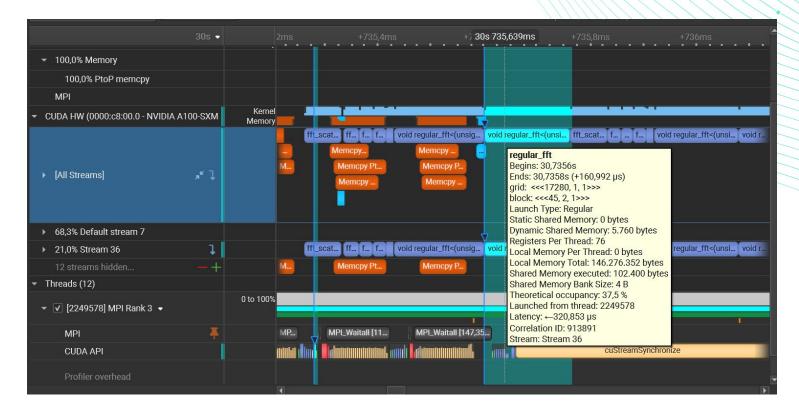
0 ns

0 ns

Delete@daxpv.f90:33

 $0 \, \mathrm{ns}$ 

#### **NVIDIA libraries**



#### Asynchronous and overlap

		Ø Options						. ı 1x		
	26s 🗸	ns	+493,2ms	+493,3ms	+493,4ms	+493,5ms	+493,6ms	+493,7ms	+493,8ms	+493,9
▶ CPU (32)		100%								Ŧ
CUDA HW (0000:c8:00.0	- 🐺	Kernel Memory							7	
21,0% Stream 36			voic regular_fft<(un	signed int) void re	egular_fft<(unsigned	int fft_scalar_cuf	ft_cft_2xy_gpu_29	ff f f f	void regular_fft<(unsig	gned int)1
2,8% Stream 66	¥									
2,8% Stream 68	Ţ									
2,7% Stream 67	¥		Ļ							
CUDA API	Ŧ	Cu	h lahah nuniahini da h		CU	daEventSynchronize	9			
р. 										Þ

= Timeline View		Ø Options				■ Q <b>□</b>	1x		
	26s 🗸					+493,2ms			🕈 🗂
CPU (32)		100%							÷
CUDA HW (0000:c8:00.0 -	Ŧ	Kernel Memory							
21,0% Stream 36	4		void regular_fft<(unsigned int)1	8 <mark>0, EPT&lt;(unsigned int)4</mark> ,	(unsigned int)5, (unsig	ned int)9>, (unsigned int)8	, (unsigned int)3, (padding	_t)0, (twiddle_t)0, (I	oadstor
2,8% Stream 66	¥								
2,8% Stream 68	¥								
2,7% Stream 67	Ŧ								
CUDA API			fft_s fft fft	fft_sc c reg re	eg fft fft	fft fft fft	reg reg	fft fft	fft
		Ï	4						Þ

### Network usage

#### -trace=mpi --nic-metrics=true

			e q 🔍	1x (i) <u>15 mess</u>
24s 🗸				
▼ [1511782] MPI Rank 1 ▼				
MPI	MPLWait [1	MPI_Wait [176,297 ms]	J	MPL_Wait [173,945 ms]
CUDA API				
Profiler overhead				
✓ [1511808] async	0 to 100%			
9 threads hidden+	0 to 100%			
<ul> <li>NIC 0 (mlx5_0 - NVIDIA ConnectX-6)</li> </ul>	ا ـــــا	الالبابا بالالبابات	allaslalala	والمرابع المرابع المرابع المرابع
IPolB: Bytes received	0 to 4.75 MiB/s			
IPolB: Bytes sent	0 to 741 kiB/s			
IB: Bytes received	0 to 84.5 GiB/s	al fact at the fact at the fact	atinitinii	aluciatioiuciatioiuci.
IB: Bytes sent	0 to 97.2 MiB/s			
IPoIB: Avg. sent packet size	0 to 208 B			
IPolB: Avg. received packet size	0 to 457 B			
IB: Avg. sent packet size	0 to 627 B			
IB: Avg. received packet size	0 to 120 kiB			
▶ NIC 1 (mlx5_1 - NVIDIA ConnectX-6)	الماعداء ا	aliicla Lielicla Lielici	atisijsiatjelj	بالالداء الداريا البليدان

#### **MPI** awareness

		1x <u>1 error, 14 messag</u>
46s •	+556ms +556,05ms +556,1m	
100,0% PtoP memcpy	Memcpy PtoP (destination)	Memcpy PtoP (destination)
MPI	MPI_Allreduce [214,721 µs	
✓ CUDA HW (0000:56:00.0 - NVIDIA A100-SXM-C Kernel Memory		
100,0% PtoP memcpy	Memcpy PtoP (destination)	Memcpy PtoP (destination)
MPI	MPI_Allreduce [205,024 µs]	
✓ CUDA HW (0000:8f:00.0 - NVIDIA A100-SXM-6 Memory		
100,0% PtoP memcpy	Memcpy PtoP (destination)	Memcpy PtoP (destination)
МРІ	MPI_Allreduce [213,952 µs]	
CUDA HW (0000:c8:00.0 - NVIDIA A100-SXM-6 Kernel Memory		
▶ [All Streams]	Memcpy PtoP (source) Memcpy PtoP (source) Memcpy PtoP (source)	Memcpy PtoP (source) Memcpy PtoP (source) Memcpy PtoP (source)
MPI 🖡	MPLAllreduce [245,275 µs]	



#### CINECA

We acknowledge **OpenACC.org** and **NVIDIA** for fruitful learning and training material